

CURRICULLUM VITAE

TARANDIP SINGH

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OBJECTIVE:

Intend to build a career in teaching with leading institute of hi-tech environment with committed & dedicated people, which will help to explore myself fully and realize my potential. Willing to work as a key player in challenging & creative environment.

EDUCATION:

- **M.Tech (ECE)** securing **8.09 CGPA** from Dr B. R. Ambedkar National Institute of Technology, Jalandhar in July 2009.
- **B.Tech (ECE)** securing **71.08%** from Baba Banda Singh Bahadur Engg. College, Fatehgarh Sahib in May 2004.
- **Diploma (ECE)** securing **65.28%** from Govt. Polytechnic Guru Teg Bahadur Garh, Moga in May 2000.
- **Matriculation** securing **70.61%** from Dhudial Khalsa Senior Secondary School, Patiala in March 1997.

PROJECT UNDERTAKEN:

- **Diploma Project:** Automatic Voltage Stabilizer.
- **B.Tech Project:** Versatile Industrial Timer using 8051 microcontroller.
- **M.Tech Thesis:** Optimization of FIR Filter using RAG Algorithm.

COMPUTER PROFICIENCY:

General: MS-Office, Internet.
Programming: VHDL, C, C++, Assembly 8051.
Others: Protues Simulator.

TRAINING EXPERIENCE:

- **6 months Industrial Training** done at **Reliance Infocomm Ltd., MCN Patiala** in the ISP Department under the able guidance of Mr.Vinayak Chopra(MCN In charge). Having knowledge of Transmission equipments (TN-1C, TN-1X) and their maintenance.
- Undergone two weeks industrial training at E10B, BSNL PATIALA (twice).

TEACHING EXPERIENCE:

TOTAL EXP.: 5 yrs.

- Presently serving as Assistant Prof. at **Sri Guru Granth Sahib World University, Fatehgarh Sahib** since January-2012.
- Served as Assistant Prof. at **RIMT-Maharaja Aggrasen Engg. College, Mandi Gobindgarh** from July-2009 to January-2012.
- Served as lecturer at **Dr B. R. Ambedkar National Institute of Technology, Jalandhar** from August-06 to December-06 and from January 2007 to June-07.
- Served as lecturer at **Thapar Polytechnic College, Patiala** from January-06 to May-06.

PUBLICATIONS:

Book:

- Tarandip Singh, Indu Saini “**Optimization Techniques for FIR Filter**”, LAP Lambert Academic Publishing, Germany, ISBN: 978-3-659-17618-0.

International Conference:

- Tarandip Singh, Indu Saini “**Area and Speed optimization of FIR filter**”, International conference on wireless networks and embedded systems, WECON-09, CIET, Rajpura, Punjab, India.

WORKSHOPS AND CONFERENCES:

- Workshop on VLSI Design during 22nd International conference on VLSI design-2009, New Delhi, India.
- Workshop on Ethical Hacking and Information Security- 2009 conducted by Kyrion digital securities, New Delhi, India.

FACULTY DEVELOPMENT PROGRAMME:

- FDP sponsored by Dept. of Science and Technology, Govt. of India, New Delhi from 15th December 2009 to 23rd December 2009.
- FDP sponsored by PTU, Jalandhar from 27th June 2010 to 1st July 2010.

AREA OF INTEREST:

- Digital VLSI Design
- Nanoelectronics

PERSONAL DETAIL:

FATHER’S NAME: S.Kuldip Singh
MOTHER’S NAME: Smt.Paramjit Kaur
DATE OF BIRTH: 22-10-1982
BIRTH PLACE: Patiala
STATE OF DOMICILE: Punjab
NATIONALITY: Indian

DECLARATION:

I consider myself to be having good knowledge about Electronics & Communication Engineering aspects. I hereby declare that the information furnished above is true to the best of my knowledge.

(Tarandip Singh)