JAPNEET KAUR
(Assistant Professor)
Department of Electronics Engineering
SGGSWU, FATEHGARH SAHIB, INDIA

M.TECH in VLSI Design
NIT, Kurukshetra

B.TECH in Electronics and Communication Engineering
Kurukshetra University

Area of Specialisation – Digital VLSI design

Teaching and Work Experience (5 years teaching experience)

Presently working with Sri Guru Granth Sahib World University since August 2013

Publications

- Paper on Fault Tolerance of FPGAs via Partial Reconfiguration in National Level Technical Paper Presentation at NIT, Kurukshetra.
- Paper on Global Clock Distribution Using Coupled Standing–Wave Oscillators in National Level Technical Paper Presentation at NIT, Kurukshetra.
- Paper on Low Power Clock Distribution using Injection-Locked Clocking in National Level Technical Paper Presentation at Kurukshetra University, Kurukshetra.
- Paper on "Design and Implementation of Advanced Majority Voter for Enhanced Fault Tolerance in Digital Circuits" National Conference of Emerging Horizons in Science and Technology 2014, SGGSWU, Fatehgarh Sahib.
- Paper on MIMO OFDM in Wimax in National Conference of Emerging Horizons in Science and Technology 2014, at SGGSWU, Fatehgarh Sahib.
- Paper on Enhancement of Multi-Channel UART using BIST Technique in National Conference of Emerging Horizons in Science and Technology 2014, at SGGSWU, Fatehgarh Sahib

Short Term Courses

- Short term training program on Digital Signal Processing: Concepts and Applications at GNDEC, Ludhiana.

- Short term training program on Wireless Communication at NITTTR, Chandigarh.

- Short term faculty development program on ‘Communication Skills: Key to Effective Teaching’ at Amity University, Uttar Pradesh.

- Short term faculty training program on ‘Academic Planning for Program Excellence’ at Amity University, Uttar Pradesh.

Software Proficiency

Hardware description Language: Verilog, VHDL
Hardware Simulation Tools : ELDO, SPICE, Modelsim
Application Software : Xilinx ISE